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[SPECIFICATION]

[TITLE OF THE INVENTION]

APPARATUS AND METHOD FOR CLASSIFYING OUTPUT SYMBOLS OF AN INTERLEAVER IN A MOBILE COMMUNICATION SYSTEM

[BRIEF DESCRIPTION OF THE DRAWINGS]

FIG. 1 is a block diagram of a channel transmitting device according to an embodiment of the present invention.

FIG. 2 is a diagram illustrating input order of symbols inputted to a first interleaver when a coding rate is 1/3, in a channel transmitting device according to an embodiment of the present invention.

FIG. 3 is a diagram illustrating output order of symbols interleaved and outputted when a coding rate is 1/3 and a frame size is 20-ms, in a channel transmitting device according to an embodiment of the present invention.

FIG. 4 is a diagram illustrating output order of symbols interleaved and outputted when a coding rate is 1/3 and a frame size is 40-ms, in a channel transmitting device according to an embodiment of the present invention.

FIG. 5 is a diagram illustrating output order of symbols interleaved and outputted when a coding rate is 1/3 and a frame size is 80-ms, in a channel transmitting device according to an embodiment of the present invention.

FIG. 6 is a block diagram illustrating an example of a symbol classifier for classifying output symbols of a first interleaver when a coding rate is 1/3, in a channel-transmitting device according to an embodiment of the present invention.

FIG. 7 is a block diagram illustrating another example of a symbol classifier for classifying output symbols of a first interleaver when a coding rate

is 1/3, in a channel-transmitting device according to an embodiment of the present invention.

FIG. 8 is a block diagram illustrating still another example of a symbol classifier for classifying output symbols of a first interleaver when a coding rate is 1/3, in a channel-transmitting device according to an embodiment of the present invention

FIG. 9 is a diagram illustrating input order of symbols inputted to a first interleaver when a coding rate is 1/2, in a channel transmitting device according to an embodiment of the present invention.

FIG. 10 is a diagram illustrating output order of symbols interleaved and outputted when a coding rate is 1/2 and a frame size is 20-ms, in a channel transmitting device according to an embodiment of the present invention.

FIG. 11 is a diagram illustrating output order of symbols interleaved and outputted when a coding rate is 1/2 and a frame size is 40-ms, in a channel transmitting device according to an embodiment of the present invention.

FIG. 12 is a diagram illustrating output order of symbols interleaved and outputted when a coding rate is 1/2 and a frame size is 80-ms, in a channel transmitting device according to an embodiment of the present invention.

FIG. 13 is a block diagram illustrating a symbol classifier for classifying output symbols of a first interleaver when a coding rate is 1/2, in a channel-transmitting device according to an embodiment of the present invention.

FIG. 14 is a block diagram illustrating an apparatus for classifying output symbols from a first interleaver into a systematic information part and a parity part and rate-matching them in different puncturing patterns when a coding rate is 1/2, in a channel transmitting device according to an embodiment of the present invention.

[DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT]

[OBJECT OF THE INVENTION]

[RELATED FIELD AND PRIOR ART OF THE INVENTION]

The present invention relates generally to a channel transmitting apparatus in a mobile communication system, and in particular, to an apparatus and method for classifying output symbols of a channel interleaver into a systematic information part and a parity part to perform rate matching.

The present invention relates to a rate-matching apparatus and method for increasing data transmission efficiency of a channel coding scheme and improving system performance in a multiple-access/multiple-channel technique in a mobile communication system such as a satellite system, ISDN (Integrated Services Digital Network), a digital cellular system, W-CDMA (Wideband-Code Division Multiple Access), UMTS (Universal Mobile Telecommunication System), and IMT (International Mobile Telecommunication)-2000. In particular, the present invention relates to an output of a channel interleaver, that is, a relation between interleaver's operation and rating matching. Has not yet been proposed a method for rate matching, according to a transmission rate, symbols channel-encoded through a turbo code in a multiple-access/multiple-channel system. The rate matching has recently emerged as a significant issue to the UMTS to increase data transmission efficiency in the air interface and improve system performance. Therefore, for properly performing the rate matching, the present invention proposes a method for properly classifying channel-interleaved symbols. The method relates to an error correction code for increasing reliability of a digital communication system, and can improve system performance of the conventional digital communication system and a mobile communication system such as UMTS and CDMA-2000.

In a conventional mobile communication system such as a satellite system, ISDN (Integrated Services Digital Network), a digital cellular system, W-CDMA (Wideband-Code Division Multiple Access), UMTS (Universal Mobile Telecommunication System), and IMT (International Mobile Telecommunication)-2000, a convolutional code and a linear block code using a single decoder are mainly used for a channel encoding method. In a multiple-access/multiple-channel system using this channel encoding method, a rate-matching principle for increasing data transmission efficiency of a channel coding scheme and system performance has been developed. However, this rate-matching principle is based on the assumption that a convolutional code, a linear block code, or a concatenated code using a convolutional code is used as a channel code. Some generalized rate-matching methods have been already proposed for these codes. But, in the case of using a turbo code as a channel code, a rate-matching method for increasing data transmission efficiency of a channel coding scheme and system performance in a multiple-access/multiple-channel system has not been developed as yet. In particular, since the turbo code has a new characteristic different from that of a convolutional code and a general linear block code, the data transmission efficiency and system performance cannot be easily improved through a conventional rate-matching method when the turbo code is used instead of the convolutional code and the general linear code. Therefore, a new rate-matching method is required.

When a linear block code is used (a convolutional encoder and a single decoder are used in this case), the following requirements of rate matching should be satisfied to increase data transmission efficiency and system performance in a multiple-access/multiple-channel scheme.

1. An input symbol sequence is punctured/repeated in a predetermined

periodic pattern.

2. The number of punctured symbols is minimized whereas the number of repeated symbols is maximized.

3. A uniform puncturing/repeating pattern is used to puncture/repeat encoded symbols uniformly.

The above requirements are set on the assumption that the error sensitivity of a code symbol output from a convolutional encoder is similar at any position in one frame. Although some favorable results can be produced in the above method, a different rate matching scheme should be employed to use a turbo encoder, including a PCCC (Parallel Concatenated Convolutional Code) and an SCCC (Serially Concatenated Convolutional Code), due to a different error sensitivity of a symbol at a different position in one frame, unlike the convolutional encoder.

Problems of the conventional art can be summarized as follows.

1. A rate-matching method used for a conventional convolutional code and linear block code is base on the assumption that the error sensitivity of a code symbol outputted from an encoder is similar at any position in one frame. However, since this assumption cannot be made in case of the turbo code, new conditions for rate matching is required for the turbo code.

2. As shown above, in the case of using the turbo code, symbols outputted from a channel encoder can be divided into a systematic information part and a parity part for optimal rate matching. In addition, even when additional

processes are added between channel interleavers, symbols outputted from a channel encoder can be divided into a systematic information part and a parity part for optimal rate matching so as to optimally perform rate matching.

3. However, since input symbol order of an interleaver is randomly varied after interleaving, symbols outputted from a channel encoder cannot be divided into a systematic information part and a parity part. Therefore, rate matching cannot be optimally performed in this case.

[SUBSTANTIAL MATTER OF THE INVENTION]

It is, therefore, an object of the present invention to provide a rate-matching apparatus and method capable of dividing an interleaver's respective output symbols into a systematic information symbol and a parity symbol according to their respective properties even though input symbol order of the interleaver is randomly varied after interleaving, in a mobile communication system that uses a part or all of a convolution code and a linear block code and a turbo code.

To achieve the above objects, there is provided a channel encoding apparatus in a mobile communication system. The channel encoding apparatus comprises an encoder for encoding frame data to generate at least two symbol groups, an interleaver for interleaving the symbol groups received from the encoder and a symbol classifier for demultiplexing the interleaved symbols from the interleaver to generate the symbol groups.

[CONSTRUCTION AND OPERATION OF THE INVENTION]

A purpose of using a component rate matcher is to increase data transmission efficiency of a channel encoding technique and to improve system performance in a multiple-access/multiple-channel method in a mobile communication system. Rate matching refers to control of input bit number to output bit number through puncturing when the input size is larger than the output size or repetition when the input size is smaller than the output size. The symbol puncturing or repetition is generally performed periodically but the followings should be considered for rate matching when a turbo code is used.

Conditions for Turbo Code Puncturing Method

1. Because the turbo code is a systematic code, a systematic information symbol part of encoded symbols should be excluded from puncturing. In addition, since an iterative decoder is used as a decoder for a turbo code, the systematic information symbol part should be excluded form puncturing.

2. A minimum free distance between final codes preferably maximizes that of each component encoder since two component encoders are connected in parallel in a turbo encoder due to the nature of the turbo code. Therefore, the output symbols of the two component encoders should be equally punctured to achieve optimal performance.

3. Because, in case of most iterative decoders, decoding is firstly performed through a first internal decoder, a first output symbol of a first component encoder should be excluded from puncturing.

4. In addition, output symbols of respective component encoder should be uniformly punctured through a uniform puncturing pattern, as in a

conventional nonsystematic convolutional code.

5. In consideration of decoder's performance, termination tail bits used in a turbo code encoder should be repeated. That is, in case of using a specific decoder such as a SOVA (Soft Output Viterbi Algorithm) decoder, decoding performance varies according to a puncturing pattern of the termination tail bits.

Conditions for Turbo Code Repeating Method

1. Because the turbo code is a systematic code, a systematic information symbol part of encoded symbols should be preferably repeated to increase symbol energy. In addition, since an iterative decoder is used as a decoder for a turbo code, the systematic information symbol part should be frequently repeated.

2. A minimum free distance between final codes preferably maximizes that of each component encoder since two component encoders are connected in parallel in a turbo encoder due to the nature of the turbo code. Therefore, in case of repeating a parity symbol, the output symbols of the two component encoders should be equally repeated to achieve optimal performance.

3. Because, in case of most iterative decoders, decoding is firstly performed through a first internal decoder, a first output symbol of a first component encoder should be preferentially repeated, in case of repeating a parity symbol.

4. In addition, output symbols of respective component encoder should be uniformly repeated through a uniform repeating pattern, as in a conventional nonsystematic convolutional code.

5. In consideration of decoder's performance, termination tail bits used in a turbo code encoder should not be punctured. That is, in case of using a specific decoder such as a SOVA (Soft Output Viterbi Algorithm) decoder, decoding performance varies according to a repeating pattern of the termination tail bits.

As described above, in the case of using the turbo code, symbols outputted from a channel encoder can be divided into a systematic information part and a parity part for optimal rate matching. In addition, even when additional processes are added between channel interleavers, symbols outputted from a channel encoder can be divided into a systematic information part and a parity part for optimal rate matching so as to optimally perform rate matching. However, since input symbol order of an interleaver is randomly varied after interleaving, symbols outputted from a channel encoder cannot be divided into a systematic information part and a parity part. Therefore, rate matching cannot be optimally performed in this case. Therefore, after these problems are solved, optimal rate matching can be embodied. For example, a channel structure used in an uplink channel of the UMTS will be described below.

Referring to FIG. 1, in case of an uplink channel, a first interleaver 112 and a radio frame segmenter 113 exist between a channel encoder 111 and a rate matcher 114. The first interleaver 112 performs interleaving according to a transmission time and the number of input bits. The radio frame segmenter 113 segments a frame inputted at a transmission time unit into 10-ms blocks and outputs them sequentially. Therefore, whether symbols outputted from the channel encoder 111 can be divided into a systematic information part and a parity part depends on a distribution property of respective output symbols from the channel encoder 111, which is determined by the first interleaver 112.

A preferred embodiment of the present invention will be described herein below with reference to the accompanying drawings, wherein like numbers designate like objects. In the following description, well-known functions or constructions are not described in detail since they would obscure the invention in unnecessary detail.

First, a description will be made of an interleaving algorithm of the first interleaver 112 used in a conventional UMTS uplink channel and then a characteristic of the interleaving algorithm. Next, there will be given a description of a method for dividing symbols transmitted from the channel encoder 111 to the first interleaver 112 into a systematic information part and a parity part using the characteristic.

Operation and Algorithm of First Interleaver

A description will be hereinbelow made of a first interleaver used in a conventional uplink channel. Four types of interleavers are currently used. And an interleaving method is comprised of the following two steps. A first step is an operation of writing an output symbol of a channel encoder in an interleaver's memory, that is, a write mode. A second step is an operation of reading out a symbol written in the interleaver's memory, that is, a read mode. The write mode and the read mode are described below on the assumption that a coding rate (R) of the channel encoder is 1/3.

First Step: WRITE MODE

1. The total number of columns (C1) is determined referring to Table 1 shown below.

2. A minimum integer R1, which is the number of rows, is found in an equation given by

$$K1 \leq R1 \times C1 \qquad \ldots\ldots (1)$$

where R1 is the number of rows and K1 is the length of an input frame.

3. The first interleaver input sequence is arranged by rows in an rectangular array having R1 rows and C1 columns.

Here, after one row is completely filled, a following row is subsequently filled.

Second Step: READ MODE

1. Columns are reordered according to an inter-column permutation pattern $\{P1(j)\}$ $(j = 0, 1, \ldots, C-1)$ shown in Table 1. $P1(j)$ represents the original column of a j^{th} permuted column and the pattern is derived in a bit reverse method where a bit sequence indicating the index of a column is relocated to indicate the index of another column in a reverse order.

2. The first interleaver output is a sequence resulted from reading the permuted $R_1 \times C_1$ array by columns. Bits that do not exist in the 1st-interleaver input are excluded from outputting by eliminating I_1 defined as

$$I1 = R1 \times C1 - K1 \qquad \ldots\ldots (2)$$

(Table 1)

Interleaving span	Total number of columns	Inter-column permutation patterns
10ms	1	{0}
20ms	2	{0, 1}
40ms	4	{0, 2, 1, 3}
80ms	8	{0, 4, 2, 6, 1, 5, 3, 7}

As a result of the two steps, an output of the first interleaver 112 is grouped in accordance with an input symbol group. That is, if a value determined by performing modulo operation with 3 on input symbol order k (k = 0, 1, 2, ···) of the first interleaver 112 is 0, then the input symbol is labeled as "s (Systematic information symbol part)". If the value is 1, then the input symbol is labeled as "p1 (Parity symbol part 1)". If the value is 2, then the input symbol is labeled as "p2 (Parity symbol part 2)". If symbols are inputted as follows.

s p1 p2, s p1 p2, s p1 p2, s p1 p2, s p1 p2, ······.

Then, an output pattern of the first interleaver 112 is the same as an output pattern of the channel encoder 111, that is, s, p1, p2, s, p1, p2, ···(or s, p2, p1, s, p2, p1, ···). Bit output order is the same as bit input order in the radio frame segmenter 113. Therefore, it is possible to divide the bits into respective parts using a demultiplexing structure at an output side of the radio frame segmenter in an uplink channel. Here, bit order within each component group changes, as compared to a downlink channel, which does not matter. By performing rate matching on an information part and a parity part each as described above, system performance can be improved. This operation will be described below in detail.

First, let input symbols of the interleaver be distinctively labeled as follows.

Systematic information part's bit (s): □ (blank rectangle)

Parity part 1's bit (p1): Ⅲ (rectangle marked with slant lines)

Parity part 2's bit (p2): ■ (rectangle marked black)

FIG. 2 illustrates sequential input symbols of the first interleaver when an interleaver size is 160 bits and a coding rate is 1/3.

In FIG. 2, the interleaver sequentially receives code symbols 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, ···, 160. Each number represents an encoded bit received from the channel encoder 111. In view of the nature of a turbo code, the first interleaver output follows the pattern of s, p1, p2, s, p1, p2, s, p1, ···, p2.

When a frame size is 20-ms, output symbols follow an interleaved order of 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, ···, 160, that is, a pattern of s, p2, p1, s, p2, p1, s, p2, ···, p1 shown in FIG. 3. Therefore, a symbol position within the pattern before interleaving is identical to that within the pattern after interleaving. That is, output symbols after interleaving can be divided into respective parts, as in case of input symbols.

When a frame size is 40-ms, output symbols follow an interleaved order of 1, 5, 9, 13, 17, 21, 25, 29, 33, ···, 160, that is, a pattern of s, p1, p2, s, p1, p2, s, p1, ···, p2 shown in FIG. 4. Therefore, a symbol position within the pattern before interleaving is identical to that within the pattern after interleaving, as in case of 20-ms. That is, output symbols after interleaving can be divided into respective parts, as in case of input symbols.

When a frame size is 80-ms, output symbols follow an interleaved order of 1, 9, 17, 25, 33, 41, 49, 57, 65, ···, 160, that is, a pattern of s, p2, p1, s, p2, p1, s, p2, ···, p1 shown in FIG. 5. Therefore, a symbol position within the pattern before interleaving is identical to that within the pattern after interleaving. That is, output symbols after interleaving can be divided into respective parts, as in case of input symbols.

As described in the foregoing examples, an output pattern of interleaved

symbols maintains the sequence of s, p1, p2, s, p1, p2, ··· (or s, p2, p1, s, p2, ···). Therefore, by performing rate matching according to respective parts, optimal system performance can be obtained.

< Output Symbol Classifier of First Interleaver>

FIGs. 5, 6 and 7 illustrate a device for classifying symbols corresponding to respective groups from the first interleaver 112. Since a symbol classifier performs modulo operation with n on an output symbol, it can be easily embodied through n-DEMUX. The parity part 1 is exchanged for the parity part 2 according to a frame size (time interval), which can be adjusted according to circumstances. In FIG. 5, since the parity part 1 is not discriminated from the parity part 2 in general, discrimination may not be necessary regarding a parity part. In addition, if discrimination is necessary, a symbol classifier may discriminate a parity part 1 from a party part 2, as shown in FIGs. 6 and 7. As described above, output symbols can be classified through a very simple hardware structure, that is, a DEMUX alone. Therefore, this structure can be applied to a case that a turbo code is used in a UMTS uplink, as suggested above.

FIG. 6 illustrates a case where a parity part 1 and a parity part 2 are not discriminatively outputted, and FIGs. 7 and 8 illustrate another case where a parity part 1 and a parity part 2 are discriminatively outputted. In addition, FIG. 7 illustrates a case where output symbols of a symbol classifier (DEMUX) 62 are outputted in the pattern of s, p1, p2, s, p1, p2, ······, and FIG. 8 illustrates another case where output symbols of a symbol classifier (DEMUX) 62 are outputted in the pattern of s, p2, p1, s, p2, p1, ······. Since structures in respective cases are the same in operation, the operation will be described in detail with reference to FIG. 6 as an example.

Referring to FIG. 6, an encoder 60 encodes an input information bit (Ik). Here, for example, the encoder 60 can be a turbo coder, and a coding rate of the encoder 0 is assumed to be 1/3. A first interleaver 61 interleaves encoded symbol data outputted from the encoder 60. Here, interleaved symbol data outputted from the first interleaver 61 follow the pattern of s, p1, p2, s, p1, p2, ······, according to the properties of the first interleaver 61. The symbol classifier 62 performs modulo operation with 3 on input order of symbols received from the first interleaver 61. If the result of the modulo operation is 0, then the classifier 62 outputs a corresponding symbol to a first terminal. If 1, then the classifier 62 outputs a corresponding symbol to a second terminal. If 2, then the classifier 62 outputs a corresponding symbol to a third terminal. Here, the symbol outputted to the first terminal is a symbol corresponding to an information bit, and the symbols outputted to the second and third terminals are symbols corresponding to parity bits. Here, the order of the parity parts 1 and 2 may vary according to a frame size (time intervals, for example, 10-ms, 20-ms, 40-ms and 80-ms). In general, as shown in FIG. 6, the parity part 1 is not discriminated from the parity part 2. If discrimination is necessary, the parity parts 1 and 2 are discriminatively outputted, as shown in FIGs. 7 and 8. In FIG. 7, an output of the symbol classifier 62 comprises a information part, a parity part 1 and a parity part 2. In FIG. 8, an output of the symbol classifier 62 comprises a information part, a parity part 2 and a parity part 1. For example, a case where a frame size is 40-ms corresponds to FIG. 7, and another case where a frame size is 10-ms, 20-ms or 80-ms corresponds to FIG. 8. Here, the symbol classifier 62 may exist between the first interleaver 112 and the radio frame segmenter 113 in the channel transmitting device of FIG. 1, or between the radio frame segmenter 113 and the rate matcher 114. In embodiments of the present invention, the symbol classifier 62 exists between the first interleaver 112 and the radio frame segmenter 113.

As another example, a symbol-classifying device will be described below, wherein a turbo interleaver size is 160 bits and a coding rate of a turbo code is 1/2.

FIG. 9 shows input order of symbols outputted from a turbo coder of a coding rate 1/2 being inputted to an interleaver. Here, the input order of the interleaver follows a sequential pattern of 1, 2, 3, 4, ···, 160. In view of the nature of a turbo code, input symbols follow the pattern of s (information symbol), p (parity symbol), s, p, ···, p.

In connection with respective frame sizes, patterns of symbols outputted after interleaving will be described herein below.

FIG. 10 illustrates order of symbols outputted after interleaving when a frame size is 20-ms. When a frame size is 20-ms, symbols inputted to an interleaver are sequentially written in a memory of row size (R) 80 and column size (C) 2, read out by rows in a read mode. Therefore, output symbol order follows the pattern of 1, 3, 5, ···, 159, 2, 4, ···, 158, 160, as shown in FIG. 8. Here, {1, 3, 5, ···, 159} are information symbols, and {2, 4, ···, 160} are parity symbols. That is, symbols outputted after interleaving can be divided into a former systematic information part and a latter parity part.

FIG. 11 illustrates order of symbols outputted after interleaving when a frame size is 40-ms. When a frame size is 40-ms, symbols inputted to an interleaver are sequentially stored in a memory of row size (R) 40 and column size (C) 4, read out by rows in a read mode. Therefore, output symbol order follows the pattern of 1, 5, 9, ···, 160, as shown in FIG. 9. Here, {1, 5, 9, ···, 159} are information symbols, and {2, 6, 10, 14, ···, 160} are parity symbols. That is,

symbols outputted after interleaving can be divided into a former systematic information part and a latter parity part.

FIG. 11 illustrates order of symbols outputted after interleaving when a frame size is 80-ms. When a frame size is 80-ms, symbols inputted to an interleaver are sequentially written in a memory of row size (R) 20 and column size (C) 8, read out by rows in a read mode. Therefore, output symbol order follows the pattern of 1, 9, 17, 25, ⋯, 160, as shown in FIG. 10. Here, {1, 9, 17, ⋯, 159} are information symbols, and {2, 10, 18, ⋯, 160} are parity symbols. That is, symbols outputted after interleaving can be divided into a former systematic information part and a latter parity part.

As described above, when a coding rate is 1/2, symbols outputted after interleaving are divided into a former systematic information part and a latter parity part, irrespective of frame sizes. In conclusion, the symbol classifier can easily perform symbol classification by dividing symbols outputted from the interleaver into two equal parts and outputting the former part and the latter part to a first output terminal and a second output terminal, respectively.

FIGs. 10 to 12 illustrate a method for classifying, through a DEMUX, symbols outputted from a first interleaver, when a coding rate is 1/3. That is, the symbols outputted from the first interleaver are classified through the DEMUX, when a coding rate is 1/2 as well as 1/3. Here, a case where a coding rate is 1/2 is different from another case where a coding rate 1/3, in that the DEMUX perform switching operation at every input symbols when a coding rate of 1/3, whereas the DEMUX repeating switching operation only by the half of the interleaver size (N) when a coding rate of 1/2. That is, as shown in FIGs. 10 to 12, since symbols are read out by each row vector, switching operation is performed at the half of

the frame size so as to classifying the symbols into a information part and a parity part.

FIG. 13 illustrates a device for classifying interleaved symbols, which is embodied on the basis of the foregoing. Referring to FIG. 13, an encoder 131 encodes an input information bit (Ik). Here, since a coding rate of the encoder is 1/2, one information symbol (C1k, s) and one parity symbol (C2k, p) are outputted in parallel from the encoder, in response to the input information bit (Ik). These outputted symbols are inputted to a first interleaver 132 in the pattern of s, p, s, p, ··· p. The first interleave 132 interleaves the inputted symbols according to a rule corresponding to a frame size. Order of symbols outputted from the interleaver 132 is illustrated in FIGs. 10 to 12. A symbol classifier 133 classifies the interleaved symbols into an information part and a parity part. When a coding rate is 1/2, symbols outputted from the first interleaver 132 are divided into a former systematic information part and a latter parity part. That is, according to a switching control signal (not shown), the symbol classifier 133 outputs symbols (a total of 80 symbols) corresponding to a half of the interleaver size and symbols corresponding to another half of the interleaver size to a first output terminal (C1j) and a second output terminal (C2j), respectively.

For example, when an interleaver size is 160 bits and a frame size is 20-ms, symbols outputted to the first output terminal are {1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, ···, 155, 157, 159}. When the frame size is 40-ms, the symbols outputted to the first output terminal are {1, 5, 9, 13, 17, 21, 25, 29, ···, 151, 155, 159}. When the frame size is 80-ms, the symbols outputted to the first output terminal are {1, 9, 17, 25, 33, 41, 49, ···, 143, 151, 159}. In addition, when an interleaver size is 160 bits and a frame size is 20-ms, symbols outputted to the second output terminal are {2, 4, 6, 8, 10, 12, 14, ···, 156, 158, 160}. When the

frame size is 40-ms, the symbols outputted to the second output terminal are {2, 6, 10, 14, 18, ···, 152, 156, 160}. When the frame size is 80-ms, the symbols outputted to the second output terminal are {2, 10, 18, 26, 34, ···, 144, 152, 160}. As described above, operation of the symbol classifier in the case of a coding rate of 1/2 is much simpler than that in the case of the coding rate of 1/3. That is, when the coding rate is 1/2, only one switching operation is required.

FIG. 14 illustrates a rate-matching device according to an embodiment of the present invention, which adopts the above symbol classifying method. Here, a coding rate is assumed to be 1/2.

Referring to FIG. 14, a encoder 141 encodes a input information bit (Ik) according to a coding rate (R) of 1/2 and generates encoded symbols. A first interleaver 142 interleaves the encoded symbols and generates interleaved symbols. A symbol classifier 143 outputs an information symbol (C1k) of the interleaved symbols and a parity symbol (C2k) of the interleaved symbols to a first rate matcher 144 and a second rate matcher 145, respectively.

The first rate matcher 144 punctures the encoded symbol C1k. Here, puncturing process criteria are as follows. Because a coding rate (R) is 1/2, an input symbol number (Nc) is Ncs/2. Here, 'Ncs' represents the total input symbol number. Since the information symbol C1k should not be punctured, an output symbol number (Ni) is R×Ncs. Because puncturing pattern determination parameters (a, b) are not punctured, they can be set to arbitrary constants. For example, the first rate matcher 144 can output symbols like "···111101011···".

The second rate matcher 145 punctures the encoded symbol C2k. Here, puncturing process criteria are as follows. Because a coding rate (R) is 1/2, an

input symbol number (Nc) is Ncs/2. Here, 'Ncs' represents the total input symbol number. Since the total number of symbols outputted after interleaving regarding the whole input symbols in one frame is 'Nis', the number of symbols outputted from the second rate matcher 145 after interleaving is 'Nis-R×Ncs'. Because puncturing pattern determination parameters (a, b) can be set to arbitrary integers according to a desired puncturing pattern. Determination of these integers is performed according to a puncturing pattern. For example, the parameters (a, b) can be (2, 1). For example, the second rate matcher 145 can output symbols like "···11x11x10x···". A MUX 146 multiplexes rate-matched symbols from the first and second rate-matchers 144 and 145, and generates multiplexed symbols.

[EFFECTS OF THE INVENTION]

As described above, the present invention is advantageous in that optimal rate matching can be performed by adding a symbol-classifying device to classify symbol data information symbols and parity symbols before a rate matching unit in a channel encoding device of a mobile communication system, when the information symbols should not to be punctured during rate matching.

[PATENT CLAIMS]

1. A channel encoding device in a mobile communication system, comprising:

an encoder for encoding frame data to generate at least two symbol groups;

an interleaver for interleaving the two or more symbol groups from the encoder; and

a symbol classifier for demultiplexing the interleaved symbols from the interleaver to generate the two or more symbol groups.

2. The channel encoding device of claim 1, wherein the two or more symbol groups are one information group and at least two parity groups.

3. The channel encoding device of claim 1, wherein the encoder is a turbo encoder.

4. The channel encoding device of claim 1, further comprising a rate matcher for rate matching, through different puncturing patterns, the two or more symbols generated from the symbol classifier.

5. A channel encoding device in a mobile communication system, comprising:

an encoder for encoding frame data to generate at least two symbol groups;

an interleaver for interleaving the two or more symbol groups from the encoder; and

a symbol classifier for classifying the interleaved symbols from the

interleaver into the two or more symbol groups.

6. A channel encoding method in a mobile communication system, comprising the steps of:

encoding frame data to generate at least two symbol groups;

interleaving the two or more symbol groups; and

classifying the interleaved symbols into the two or more symbol groups.

7. The channel encoding method of claim 6, wherein the two or more symbol groups are one information group and at least two parity groups.

8. The channel encoding method of claim 6, further comprising the step of rate matching the classified two or more symbol groups through different puncturing patterns.

[ABSTRACT OF THE DISCLOSURE]

[ABSTRACT]

Disclosed is a channel encoding apparatus in a mobile communication system. The channel encoding apparatus comprises an encoder for encoding frame data to generate at least two symbol groups, an interleaver for interleaving the symbol groups received from the encoder and a symbol classifier for demultiplexing the interleaved symbols from the interleaver to generate the symbol groups.

[REPRESENTATIVE FIGURE]

FIG. 6

[INDEX]

Channel Encoder, Interleaver, DEMUX, and Symbol Classifying.

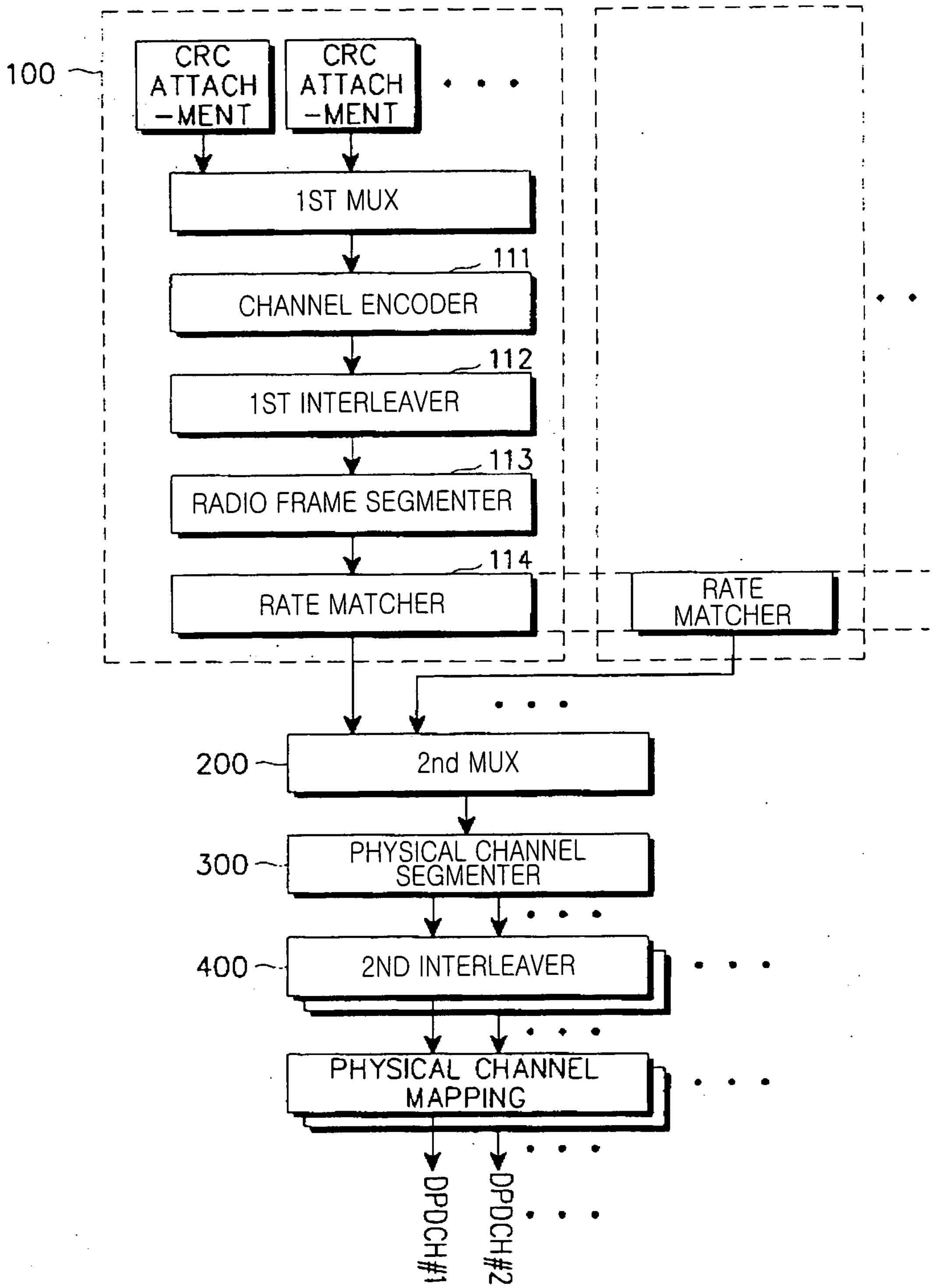
100
CRC ATTACH -MENT
CRC ATTACH -MENT
1ST MUX
111
CHANNEL ENCODER
112
1ST INTERLEAVER
113
RADIO FRAME SEGMENTER
114
RATE MATCHER
RATE MATCHER
200
2nd MUX
300
PHYSICAL CHANNEL SEGMENTER
400
2ND INTERLEAVER
PHYSICAL CHANNEL MAPPING
DPDCH#1
DPDCH#2

FIG.1

1	2	3	4	5	6	7	8
9	10	11	12	13	14	15	16
17	18	19	20	21	22	23	24
25	26	27	28	29	30	31	32
33	34	35	36	37	38	39	40
41	42	43	44	45	46	47	48
49	50	51	52	53	54	55	56
57	58	59	60	61	62	63	64
65	66	67	68	69	70	71	72
73	74	75	76	77	78	79	80
81	82	83	84	85	86	87	88
89	90	91	92	93	94	95	96
97	98	99	100	101	102	103	104
105	106	107	108	109	110	111	112
113	114	115	116	117	118	119	120
121	122	123	124	125	126	127	128
129	130	131	132	133	134	135	136
137	138	139	140	141	142	143	144
145	146	147	148	149	150	151	152
153	154	155	156	157	158	159	160

FIG.2

1	3	5	7	9	11	13	15
17	19	21	23	25	27	29	31
33	35	37	39	41	43	45	47
49	51	53	55	57	59	61	63
65	67	69	71	73	75	77	79
81	83	85	87	89	91	93	95
97	99	101	103	105	107	109	111
113	115	117	119	121	123	125	127
129	131	133	135	137	139	141	143
145	147	149	151	153	155	157	159
2	4	6	8	10	12	14	16
18	20	22	24	26	28	30	32
34	36	38	40	42	44	46	48
50	52	54	56	58	60	62	64
66	68	70	72	74	76	78	80
82	84	86	88	90	92	94	96
98	100	102	104	106	108	110	112
114	116	118	120	122	124	126	128
130	132	134	136	138	140	142	144
146	148	150	152	154	156	158	160

FIG.3

1	5	9	13	17	21	25	29
33	37	41	45	49	53	57	61
65	69	73	77	81	85	89	93
97	101	105	109	113	117	121	125
129	133	137	141	145	149	153	157
3	7	11	15	19	23	27	31
35	39	43	47	51	55	59	63
67	71	75	79	83	87	91	95
99	103	107	111	115	119	123	127
131	135	139	143	147	151	155	159
2	6	10	14	18	22	26	30
34	38	42	46	50	54	58	62
66	70	74	78	82	86	90	94
98	102	106	110	114	118	122	126
130	134	138	142	146	150	154	158
4	8	12	16	20	24	28	32
36	40	44	48	52	56	60	64
68	72	76	80	84	88	92	96
100	104	108	112	116	120	124	128
132	136	140	144	148	152	156	160

FIG.4

1	9	17	25	33	41	49	57
65	73	81	89	97	105	113	121
129	137	145	153	5	13	21	29
37	45	53	61	69	77	85	93
101	109	117	125	133	141	149	157
3	11	19	27	35	43	51	59
67	75	83	91	99	107	115	123
131	139	147	155	7	15	23	31
39	47	55	63	71	79	87	95
103	111	119	127	135	143	151	159
2	10	18	26	34	42	50	58
66	74	82	90	98	106	114	122
130	138	146	154	6	14	22	30
38	46	54	62	70	78	86	94
102	110	118	126	134	142	150	158
4	12	20	28	36	44	52	60
68	76	84	92	100	108	116	124
132	140	148	156	8	16	24	32
40	48	56	64	72	80	88	96
104	112	120	128	136	144	152	160

FIG.5

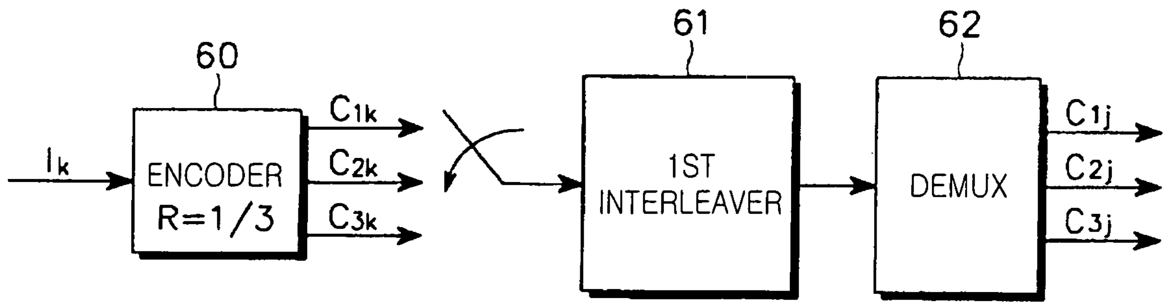

FIG.6

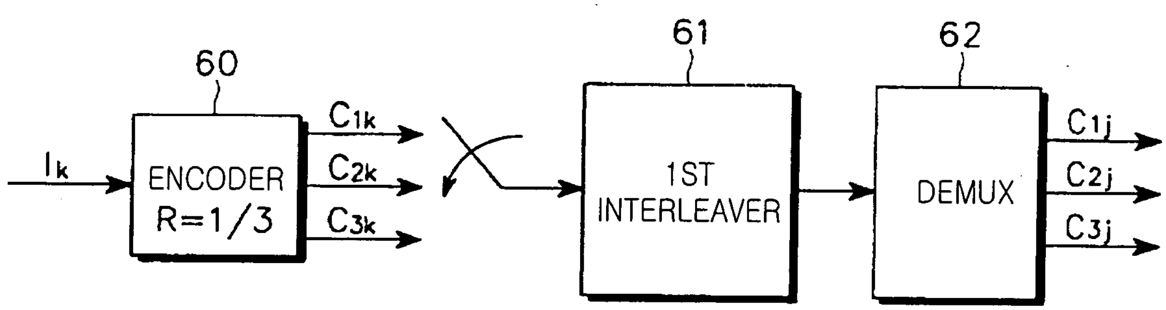

FIG.7

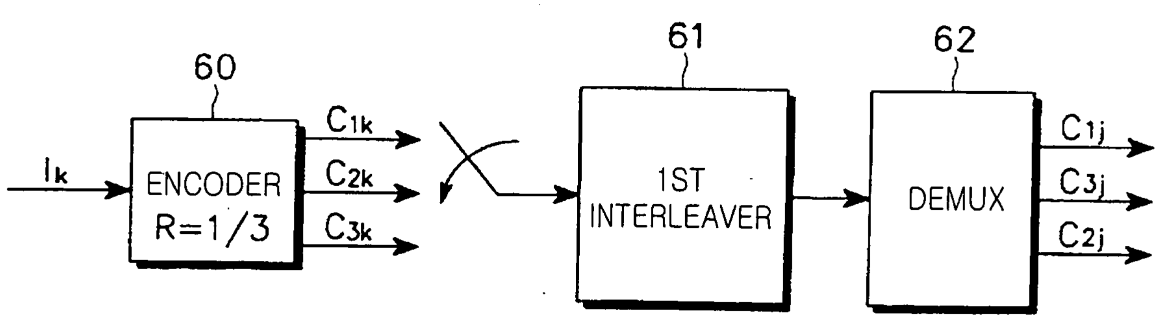

FIG.8

1	2	3	4	5	6	7	8
9	10	11	12	13	14	15	16
17	18	19	20	21	22	23	24
25	26	27	28	29	30	31	32
33	34	35	36	37	38	39	40
41	42	43	44	45	46	47	48
49	50	51	52	53	54	55	56
57	58	59	60	61	62	63	64
65	66	67	68	69	70	71	72
73	74	75	76	77	78	79	80
81	82	83	84	85	86	87	88
89	90	91	92	93	94	95	96
97	98	99	100	101	102	103	104
105	106	107	108	109	110	111	112
113	114	115	116	117	118	119	120
121	122	123	124	125	126	127	128
129	130	131	132	133	134	135	136
137	138	139	140	141	142	143	144
145	146	147	148	149	150	151	152
153	154	155	156	157	158	159	160

FIG.9

1	3	5	7	9	11	13	15
17	19	21	23	25	27	29	31
33	35	37	39	41	43	45	47
49	51	53	55	57	59	61	63
65	67	69	71	73	75	77	79
81	83	85	87	89	91	93	95
97	99	101	103	105	107	109	111
113	115	117	119	121	123	125	127
129	131	133	135	137	139	141	143
145	147	149	151	153	155	157	159
2	4	6	8	10	12	14	16
18	20	22	24	26	28	30	32
34	36	38	40	42	44	46	48
50	52	54	56	58	60	62	64
66	68	70	72	74	76	78	80
82	84	86	88	90	92	94	96
98	100	102	104	106	108	110	112
114	116	118	120	122	124	126	128
130	132	134	136	138	140	142	144
146	148	150	152	154	156	158	160

FIG. 10

1	5	9	13	17	21	25	29
33	37	41	45	49	53	57	61
65	69	73	77	81	85	89	93
97	101	105	109	113	117	121	125
129	133	137	141	145	149	153	157
3	7	11	15	19	23	27	31
35	39	43	47	51	55	59	63
67	71	75	79	83	87	91	95
99	103	107	111	115	119	123	127
131	135	139	143	147	151	155	159
2	6	10	14	18	22	26	30
34	38	42	46	50	54	58	62
66	70	74	78	82	86	90	94
98	102	106	110	114	118	122	126
130	134	138	142	146	150	154	158
4	8	12	16	20	24	28	32
36	40	44	48	52	56	60	64
68	72	76	80	84	88	92	96
100	104	108	112	116	120	124	128
132	136	140	144	148	152	156	160

FIG.11

1	9	17	25	33	41	49	57
65	73	81	89	97	105	113	121
129	137	145	153	5	13	21	29
37	45	53	61	69	77	85	93
101	109	117	125	133	141	149	157
3	11	19	27	35	43	51	59
67	75	83	91	99	107	115	123
131	139	147	155	7	15	23	31
39	47	55	63	71	79	87	95
103	111	119	127	135	143	151	159
2	10	18	26	34	42	50	58
66	74	82	90	98	106	114	122
130	138	146	154	6	14	22	30
38	46	54	62	70	78	86	94
102	110	118	126	134	142	150	158
4	12	20	28	36	44	52	60
68	76	84	92	100	108	116	124
132	140	148	156	8	16	24	32
40	48	56	64	72	80	88	96
104	112	120	128	136	144	152	160

FIG.12

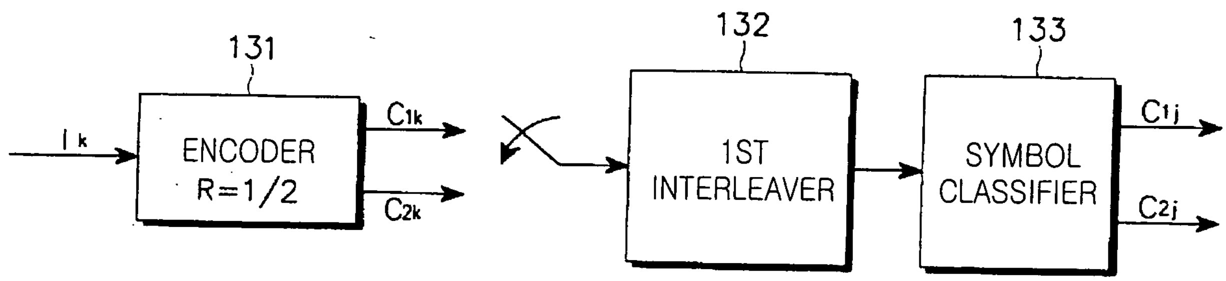
131
132
133
Ik
ENCODER
R=1/2
C1k
C2k
1ST
INTERLEAVER
SYMBOL
CLASSIFIER
C1j
C2j

FIG.13

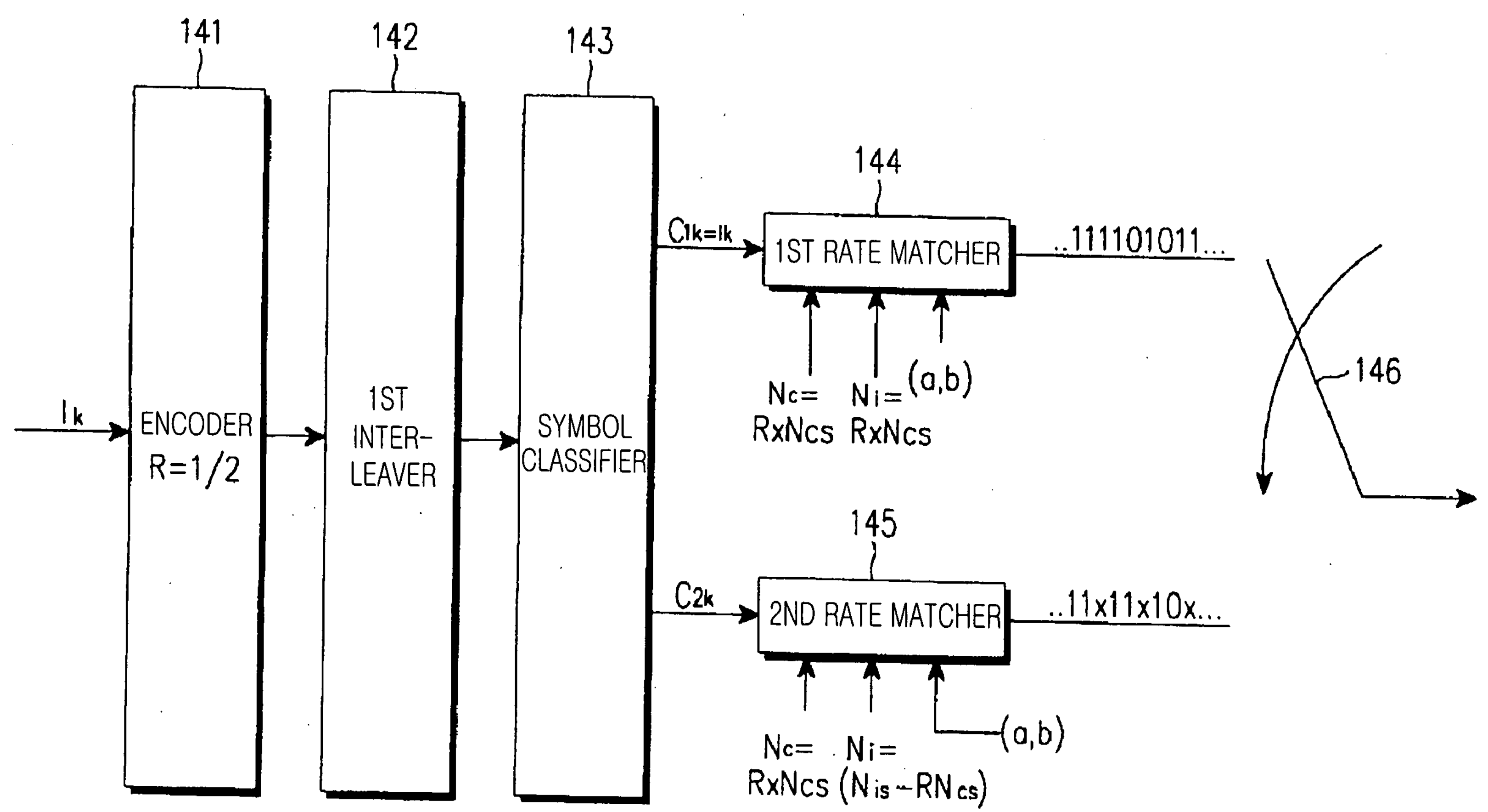
141
142
143
144
145
146
Ik
ENCODER R=1/2
1ST INTER-LEAVER
SYMBOL CLASSIFIER
C1k=Ik
C2k
1ST RATE MATCHER
2ND RATE MATCHER
..111101011...
..11x11x10x...
Nc= RxNcs
Ni= RxNcs
(a,b)
Nc= RxNcs
Ni= (Nis~RNcs)
(a,b)

FIG.14